UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,194	09/26/2003	Toshio Kimura	1035-471	4479

23117 7590 10/06/2004

NIXON & VANDERHYE, PC
1100 N GLEBE ROAD
8TH FLOOR
ARLINGTON, VA 22201-4714

EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,194	KIMURA ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	AU

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/04/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of group I (claims 1-10) in the reply filed on 07/14/04 is acknowledged.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,236,115 to Gaynes et al.

Regarding claim 1, Gaynes et al. (figures 1-9B, 13A-B) teach a chip-stack semiconductor device, comprising multiple semiconductor chips (30a, 30b, 30c) vertically stacked on top of each other, wherein:

each of the semiconductor chips (30a, 30b, 30c) includes multiple through electrodes (via electrodes are formed on both side of the chips) (column 10, lines 40-56) connected to each other in regions inside of electrode pads (33) derived from a device region, each of the through electrodes (via electrodes) linking a front surface (top surface of chip) to a back (bottom surface of chip) surface of the semiconductor chip.

Regarding claim 2, Gaynes et al. teach the electrode pads (33) are provided along a periphery of the semiconductor chip (30a, 30b, 30c) so as to surround the device region.

Regarding claim 3, Gaynes et al. teach at least one type of the through electrodes (via electrodes) is contact through electrodes electrically connected to the electrode pad (33).

Regarding claim 4, Gaynes et al. teach at least one type of the through electrodes (via electrodes) is contact through electrodes electrically connected to the electrode pad (33).

Regarding claim 5, Gaynes et al. teach at least one type of the through electrodes (middle layer [33] located on the chip [30b] or chip [30c]) is non-contact through electrodes not electrically connected to the electrode pad (right [33]).

Regarding claim 6, Gaynes et al. teach at least one type of the through electrodes (middle layer [33] is located on the chip [30b] or chip [30c]) is non-contact through electrodes not electrically connected to the electrode pad (right [33]).

Regarding claim 7, Gaynes et al. teach a through electrode (via electrode) is further provided in regions outside (via electrode is located in a distance from the middle layer [33]) of the electrode pad (middle layer [33]).

Regarding claim 8, Gaynes et al. teach a through electrode (via electrode) is further provided in regions outside (via electrode is located in a distance from the middle layer [33]) of the electrode pad (middle layer [33]).

Regarding claim 9, Gaynes et al. teach the solder (Pb, Sn), which is formed between the via electrodes of the chips. Gaynes et al. teach the pads, connections and solders, which are formed on both side of the chips (column 10, lines 40-56). Therefore, Gaynes et al. teach the through electrodes (via electrodes) in the semiconductor chips (30a, 30b, 30c) are connected to

each other via bumps (solder Pb, Sn) so that the semiconductor chips are vertically stacked on top of each other.

Regarding claim 10, Gaynes et al. teach the solder (Pb, Sn), which is formed between the via electrodes of the chips. Gaynes et al. teach the pads, connections and solders, which are formed on both side of the chips (column 10, lines 40-56). Therefore, Gaynes et al. teach the through electrodes (via electrodes) in the semiconductor chips (30a, 30b, 30c) are connected to each other via bumps (solder Pn, Sn) so that the semiconductor chips are vertically stacked on top of each other.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
September 29, 2004

DONGHEE KANG
PRIMARY EXAMINER